Concatenated Low-Density Parity-Check and BCH Coding System for Magnetic Recording Read Channel With 4 kB Sector Format

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In this paper, we examine the potential of applying concatenated low-density parity-check (LDPC) and Bose–Chaudhuri–Hocquenghem (BCH) coding for magnetic recording read channel with a 4 kB sector format. One key observation for such concatenated coding systems is that the overall error correction capability can be improved by exploiting the iteration-by-iteration bit error number oscillation behavior in case of inner LDPC code decoding failures. Moreover, assisted by field programmable gate array (FPGA)-based simulation platforms, empirical error-correcting performance analysis can reach a very low sector error rate (e.g., 10^{-10} and below), which is almost infeasible for LDPC-only coding systems. Finally, concatenated coding can further reduce the silicon cost. By implementing a high-speed FPGA-based perpendicular recording read channel simulator, we investigate a 4 kB rate-15/16 concatenated coding system with a 512-byte rate-19/20 inner LDPC code and an outer 4 kB BCH code. We apply a decoding strategy that can fully utilize the bit error number oscillation behavior of inner LDPC code decoding, and show that its sector error rate drops down to 10^{-11}. For the purpose of comparison, we use the FPGA-based simulator to empirically observe the performance of 4 kB rate-15/16 LDPC and Reed-Solomon (RS) codes down to 10^{-7}–10^{-8}. Finally, we estimate the silicon cost of this concatenated coding system at 65 nm node, and compare it with that of the RS-only and LDPC-only coding systems.

Index Terms—**Application-specific integrated circuit (ASIC), BCH, concatenated, field programmable gate array (FPGA), low-density parity-check (LDPC).**

I. Introduction

As THE conventional longitudinal recording was approaching its superparamagnetic limit [1], the new perpendicular recording technology has been quickly adopted by the industry as a promising vehicle to keep the historical areal density growth rate and approach the Tbit/in^2 areal density limit [2], [3]. It has been well recognized that achieving this promised recording density limit at reasonable cost demands innovative signal processing and error correction coding system design solutions [4]–[6]. Noticeably, there has been a great interest in replacing Reed-Solomon (RS) codes with low-density parity-check (LDPC) codes in magnetic recording channel. Meanwhile, to facilitate the development of more powerful error correction code (ECC), International Disk Drive, Equipment, and Materials Association (IDEMA) recently announced a recommendation to replace the 30-year-old 512-byte sector format with a new 4 kB sector format [7].

This work concerns the use of LDPC codes for the perpendicular recording channel with a 4 kB sector format. Due to the lack of accurate analytical methods, it remains a challenge to predict the error-correcting performance of LDPC codes in magnetic recording channel at very low sector error rates (SER) (e.g., 10^{-10} and below). Using high-speed hardware simulators based on FPGA (field programmable gate array) devices, recent work [8]–[13] has empirically investigated the performance of LDPC codes. In particular, the authors of [12] developed a simulation-assisted method to estimate the LDPC decoding performance down to 10^{-14} and lower under ideal PR channel with AWGN noise only, which has been empirically verified down to the SER of 10^{-8} using FPGA-based simulation. Even with the help of FPGA-based simulators, prior work could only empirically reach the SER down to 10^{-8}–10^{-9} for the 512-byte sector format, which is still several orders of magnitudes away from the desired SER in practice. Clearly, it would be more difficult to investigate the LDPC codes for the 4 kB sector format. As a result, the applicability of LDPC-only ECC coding solutions for magnetic recording channel still largely remains an open question.

Targeting the magnetic recording channel with the 4 kB sector format, this work focuses on concatenated coding with LDPC as the inner code and Bose–Chaudhuri–Hocquenghem (BCH) as the outer code, instead of LDPC-only coding, because of three main motivations. 1) As we will show later, LDPC code decoding failures tend to exhibit a certain degree of oscillations in terms of bit error number from one decoding iteration to the next. Such iteration-by-iteration bit error number oscillation can be leveraged by the outer BCH code to improve the overall error-correcting capability when concatenated coding systems are being used. 2) Such a concatenated coding strategy makes it possible to apply FPGA-based high-speed simulators to estimate the error-correcting performance down to very low SER (e.g., 10^{-10} and below) at a reasonably high credibility. 3) The silicon implementation cost of a concatenated coding system can be lower than that of a competing LDPC-only or RS-only coding system. The above stated features will be later demonstrated by a case study.

This paper presents a concatenated LDPC and BCH coding system design approach that fully exploits the inner LDPC code decoding oscillation behavior. To facilitate error-correcting performance estimation, we implemented an FPGA-based simulator that consists of an LDPC encoder, a perpendicular channel with media jitter and AWGN noises, an equalizer and noise predictor, a soft-output Viterbi algorithm (SOVA) detector, and an LDPC decoder. Assisted by this FPGA-based

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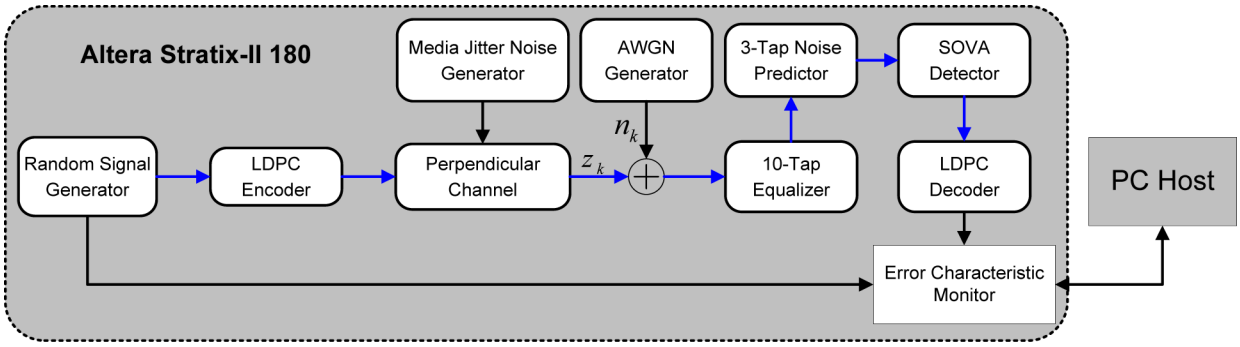

Fig. 1. FPGA-based simulation platform structure.

simulator, we demonstrate the proposed design strategy using a 4 kB rate-15/16 concatenated coding system with a 512-byte rate-19/20 inner LDPC code and an outer 4 kB BCH code. Based upon extensive empirical FPGA simulation results, estimation of SER down to 10^{-11} can be realized with a reasonably high credibility. This FPGA-based simulator is also used to empirically evaluate the performance of 4 kB rate-15/16 LDPC and RS codes down to 10^{-7}–10^{-8} for the purpose of comparison. Finally, based on application-specific integrated circuit (ASIC) design at 65 nm CMOS technology node, we evaluate the silicon cost of this concatenated coding system, which is further compared with that of the competing LDPC-only and RS-only coding systems.

The remainder of this paper is organized as follows. Section II describes the perpendicular recording read channel FPGA-based simulator used in this work. Section III presents the proposed concatenated LDPC and BCH coding system design strategy, and a case study using an inner 512-byte LDPC code for the 4 kB sector format is presented in Section IV. Conclusions are drawn in Section V.

II. FPGA-Based Simulation Platform

To facilitate the study in this work, we implemented an FPGA-based simulator using one Altera Stratix-II 180 FPGA device that contains 186 576 equivalent 4-input look-up tables (LUTs) and 9 Mb of on-chip memory. Fig. 1 shows the overall structure of this simulator. It models the perpendicular recording channel as

$$z_k = \sum_m a_m h(kT - mT + \delta_m)$$

where

$$h(t) = \mathrm{erf}(2t\sqrt{\ln 2}/(\mathrm{PW50}))$$

and the media jitter noise δ_m is modeled as a Gaussian variable $\mathcal{N}(0, \sigma_j^2)$. The parameter PW50 is defined as the pulse width of the derivative of $h(t)$ at half of its peak amplitude. We precompute 256 samples of $h(t)$, which are stored in FPGA to facilitate the realization of $h(kT - mT + \delta_m)$.

As illustrated in Fig. 1, the output of perpendicular recording channel is further disturbed by additive white Gaussian noise (AWGN) $n_k \sim \mathcal{N}(0, \sigma_n^2)$. To generate jitter noise and AWGN, we employ the quantized version of the Box-Muller method [14]. It generates a random sample x with Gaussian distribution (zero mean and standard deviation $\sigma = 1$) using two random samples x_1 and x_2 uniformly distributed between [0, 1] as follows:

$$x = f(x_1) \cdot g(x_2)$$

where

$$f(x_1) = \sqrt{-\ln(x_1)} \quad \text{and} \quad g(x_2) = \sqrt{2}\cos(2\pi x_2).$$

An array of 64-bit linear feedback shift registers is used to generate the random samples x_1 and x_2. The functions $f(x_1)$ and $g(x_2)$ are implemented using look-up tables. The random samples with the $\mathcal{N}(0, \sigma_n^2)$ distribution are scaled to generate the noises according to the following SNR definition [15]:

$$\mathrm{SNR} = \frac{\int_{-\infty}^{+\infty} (h(t) - h(t-T))^2 \mathrm{d}t}{2\sigma_n^2 + 2\sigma_j^2 \int_{-\infty}^{+\infty} (h'(t))^2 \mathrm{d}t}$$

where the signal energy is in the "dibit" response and the noise reflects the first-order jitter model.

As illustrated in Fig. 1, the read channel signal equalization/detection is realized by a 10-tap equalizer, a 3-tap noise predictor, and an SOVA detector that uses a two-step detector structure [16]. This simulation platform supports quasi-cyclic LDPC (QC-LDPC) codes. The parity check matrix $\mathbf{H}$ of a QC-LDPC code can be written as

$$\mathbf{H} = \begin{bmatrix} \mathbf{H}_{1,1} & \mathbf{H}_{1,2} & \cdots & \mathbf{H}_{1,n} \\ \mathbf{H}_{2,1} & \mathbf{H}_{2,2} & \cdots & \mathbf{H}_{2,n} \\ \cdots & \cdots & \ddots & \cdots \\ \mathbf{H}_{m,1} & \mathbf{H}_{m,2} & \cdots & \mathbf{H}_{m,n} \end{bmatrix}$$

where each submatrix $\mathbf{H}_{i,j}$ is a circulant matrix in which each row is a cyclic shift of the row above. The QC-LDPC encoder is designed using the approach proposed in [17], and the QC-LDPC decoder realizes the min-sum decoding algorithm and employs the decoder architecture presented in [18]. The finite word-length configurations of this simulation platform are outlined as follows.

TABLE I
OSCILLATION OF BIT ERROR NUMBER IN LDPC DECODING

Iteration Number	SER=4.5×10^{-6}		SER=3.7×10^{-3}	
	Failure I	Failure II	Failure I	Failure II
0	13	10	43	32
1	1	20	11	13
2	2	1	18	9
3	5	1	6	4
4	4	1	7	1
5	17	2	8	7
6	17	20	15	6
7	9	52	8	8
8	7	29	2	4

TABLE II
STATISTICS OF THE OCCURRENCE OF DIFFERENT MINIMUM BIT ERROR NUMBERS FOR THE ESTIMATION OF $P_b^{(n)}$ UNDER TWO DIFFERENT P_l

n	P_l =3.24e-6	P_l =3.91e-5
	Occurrence $\Rightarrow$ est. $P_b^{(n)}$	Occurrence $\Rightarrow$ est. $P_b^{(n)}$
1	1989 $\Rightarrow$ 1.99e-1	20021 $\Rightarrow$ 2.00e-1
2	1275 $\Rightarrow$ 1.28e-1	13644 $\Rightarrow$ 1.36e-1
3	1233 $\Rightarrow$ 1.23e-1	14645 $\Rightarrow$ 1.46e-1
4	1234 $\Rightarrow$ 1.23e-1	13111 $\Rightarrow$ 1.31e-1
5	1312 $\Rightarrow$ 1.31e-1	12345 $\Rightarrow$ 1.23e-1
6	913 $\Rightarrow$ 9.13e-2	7856 $\Rightarrow$ 7.86e-2
7	637 $\Rightarrow$ 6.37e-2	5899 $\Rightarrow$ 5.90e-2
8	423 $\Rightarrow$ 4.23e-2	3323 $\Rightarrow$ 3.32e-2
9	277 $\Rightarrow$ 2.77e-2	2523 $\Rightarrow$ 2.52e-2
10	398 $\Rightarrow$ 3.98e-2	2823 $\Rightarrow$ 2.82e-2
11	102 $\Rightarrow$ 1.02e-3	1187 $\Rightarrow$ 1.19e-2
12	90 $\Rightarrow$ 9.00e-3	1002 $\Rightarrow$ 1.00e-2
13	66 $\Rightarrow$ 6.60e-3	808 $\Rightarrow$ 8.08e-3
14	21 $\Rightarrow$ 2.10e-3	312 $\Rightarrow$ 3.12e-3
15	22 $\Rightarrow$ 2.20e-3	245 $\Rightarrow$ 2.45e-3
16	3 $\Rightarrow$ 3.00e-4	111 $\Rightarrow$ 1.11e-3
17	4 $\Rightarrow$ 4.00e-4	63 $\Rightarrow$ 6.30e-4
18	1 $\Rightarrow$ 1.00e-4	45 $\Rightarrow$ 4.50e-4
19	0	17 $\Rightarrow$ 1.70e-4
20	0	12 $\Rightarrow$ 1.20e-4
21	0	5 $\Rightarrow$ 5.00e-5
22	0	2 $\Rightarrow$ 2.00e-5
23	0	1 $\Rightarrow$ 1.00e-5
$\geq$24	0	0

1) The outputs of the perpendicular channel, AWGN generator, equalizer, and noise predictor use 6 bits.
2) The path metric and soft output of the SOVA detector use 9 bits and 3 bits, respectively.
3) The internal LDPC decoding messages use 3 bits.

Using this simulation platform, we observed significant oscillation of bit error number from one decoding iteration to the next in case of LDPC code decoding failures. This is illustrated in the following example. We constructed a regular rate-19/20 QC-LDPC code for 512-byte sectors, where the column weight of QC-LDPC code parity check matrix is 3. We set the equalization target as $1 + 0.75D$ and set the media jitter noise contribute 90% of the total noise power. At the SER of 4.5×10^{-6} and 3.7×10^{-3}, we captured two LDPC decoding failures and present the corresponding bit error numbers at each decoding iteration in Table I. Using this FPGA-based simulator, we captured many LDPC code decoding failures, all of which have the similar bit error number oscillation.

III. CONCATENATED LDPC AND BCH CODING SYSTEM

A concatenated LDPC and BCH coding system has a BCH code as the outer code and an LDPC code as the inner code, i.e., one sector of user data is first encoded by the outer BCH code encoder, then the BCH codeword is partitioned into v equal-sized segments, and each segment is encoded by the inner LDPC code encoder. Let $R_{\rm LDPC}$ and $R_{\rm BCH}$ denote the code rate of the inner LDPC code and outer BCH code, respectively, the overall code rate $R_C = R_{\rm LDPC} \cdot R_{\rm BCH}$. If all the v inner LDPC codewords are successfully decoded, we do not need to execute the outer BCH code decoding. Because of the possible LDPC code mis-correction (i.e., the LDPC decoding converges to a valid but wrong codeword), the outer BCH code may still be used to perform error detection in practice. In case of inner LDPC code decoding failure(s), we propose a simple but effective trial-and-error procedure to exploit the bit error number oscillation behavior in the presence of LDPC decoding failure to improve the overall error-correcting performance. The basic idea is that, for each LDPC code decoding failure, we use the hard decisions at different inner LDPC decoding iterations as the input to the successive BCH code decoder until the BCH code decoder succeeds or all the LDPC code decoding hard decisions have been exhausted. Let N denote the maximum iteration number of LDPC code decoding, and m denote the number of LDPC code decoding failures in one BCH codeword, we have

for $n_1 = N \cdots 0$

For the 1-st LDPC decoding failure, use the hard decision of its n_1th iteration as the decoding output.

for $n_2 = N \cdots 0$

For the 2-nd LDPC decoding failure, use the hard decision of its n_2th iteration as the decoding output.

$\vdots$

for $n_m = N \cdots 0$

For the mth LDPC decoding failure, use the hard decision of its n_mth iteration as the decoding output.

if *BCH decoding succeeds* **then**

break;

else

continue;

endif

end

$\vdots$

end

end

Let P_l denote the inner LDPC code decoding failure probability, and $P_b^{(n)}$ denote the probability that, once the LDPC code decoding fails, the minimum bit error number among all

TABLE III
ASIC DESIGN RESULTS AT 65 NM NODE

	Silicon Area (mm^2)						Throughput
	SRAM-based Buffer	LDPC Decoder	BCH Decoder	RS Decoder	Detector	Total	
Concatenated Coding	0.11	0.34	0.10	-	0.04	0.59	1Gbps
LDPC-Only	0.32	1.11	-	-	0.04	1.47	
RS-Only	0.08	-	-	0.92	0.01	1.01	

the LDPC code decoding iterations equals to n. Let t denote the error correction capability of the BCH code, the overall SER of the concatenated coding system can be estimated as

$$\sum_{m=1}^{v} \left(\binom{v}{m} \cdot (P_l)^m \cdot (1-P_l)^{v-m} \cdot S \right) \tag{1}$$

where

$$S = \sum_{\sum_{j=1}^{m} i_j > t} \left(P_b^{(i_1)} \cdot P_b^{(i_2)} \cdots P_b^{(i_m)} \right).$$

In spite of the above simple formulation, there are no existing accurate analytical methods that can estimate the values of P_l and $P_b^{(n)}$ for LDPC code decoding under magnetic recording channel. Hence, we have to empirically estimate P_l and $P_b^{(n)}$ through extensive simulations. Nevertheless, due to the very low SER requirements in magnetic recording, computer-based simulation is far less sufficient and dedicated high-speed simulators are necessary in this context.

Targeting a 4 kB sector format in magnetic recording, compared with LDPC-only ECC solutions, such a concatenated coding system design strategy makes it much more feasible to apply FPGA-based high-speed simulators to empirically estimate the error-correcting performance down to very low SERs (e.g., 10^{-10} and below). Although FPGA-based simulations have been used to evaluate the performance of LDPC-only ECC solutions, it can hardly reach sufficiently low SER for such a long sector length within a reasonable amount of simulation time. For example, suppose we use a simulator that can achieve even up to a 500 Mbps simulation throughput. To evaluate the SER down to 10^{-10} with 4 kB sector format, we need roughly 80 days, assuming we must capture about 10 LDPC decoding failures to estimate the SER. The concatenated coding system may demand much less simulation for two reasons. 1) The smaller inner LDPC codeword length directly contributes to the reduced simulation time, and more importantly, 2) empirical estimation of P_l and $P_b^{(n)}$ demands much less simulations than trying to explicitly simulate the overall system SER.

IV. CASE STUDY

In this work, we apply the FPGA-based simulator described in Section II to demonstrate the above presented concatenated coding systems. In particular, we consider a rate-15/16 4 kB concatenated coding system with the following configurations. The parity check matrix of the inner LDPC code contains an array of 3×60 circulant matrices with size of 73, where all the circulant matrices have a column weight of 1 and are constructed randomly subject to the 4-cycle free constraint. Since parity check matrix has two redundant rows, we denote the inner LDPC code as rate-19/20 (4380, 4163). Each BCH codeword is partitioned into $v = 8$ equal-sized segments, and each segment is encoded by the inner LDPC code encoder. Therefore, the codeword length of the BCH code is $8 \cdot 4163 = 33\,304$ bits. Given the overall code rate of $15/16$, we have that the information length is $8 \cdot 4380 \cdot 15/16 = 32\,850$ bits. Clearly, the outer BCH code should be constructed over $\mathrm{GF}(2^{16})$, and its maximum correctable error number t is lower bounded by $\lfloor (33\,304 - 32\,850)/16 \rfloor = 28$. By setting $t = 28$ for the worst-case scenario, we have that the outer BCH code is a (33 304, 32 850, 28) binary BCH code (note that we use (n, k, t) format to represent a linear block code, where n denotes the codeword length, k denotes the information length and t denotes the maximum number of correctable errors). The maximum number of LDPC decoding iterations is set to 8. For the FPGA-based simulator, we fix the channel bit density, which is defined as the ratio PW50/T, as 2.3, and the total noise consists of 90% media jitter noise and 10% AWGN.

As pointed out in Section III, to estimate the SER of the concatenated coding system, we apply the FPGA-based simulator to empirically estimate the inner LDPC code decoding failure rate P_l and the minimum bit error number probability $P_b^{(n)}$ in case of inner LDPC code decoding failures. Table II and Fig. 2 show the statistics of the occurrence of different minimum bit error numbers among all the inner LDPC code decoding iterations under two different inner LDPC code decoding failure rates. We note that, in all the simulations, the LDPC decoder output is always compared against with the true transmitted data, instead of relying on the parity check operation to check the convergence of decoding. Therefore, whether miscorrection occurs or not is irrelevant in this context and does not affect the results at all. Based on these empirically obtained statistic data, for the case of $P_l = 3.24 \times 10^{-6}$, it is reasonable to conjecture that $P_b^{(19)}$ and $P_b^{(20)}$ are on the order of 10^{-4}, $P_b^{(21)}$ to $P_b^{(23)}$ are on the order of 10^{-5}, $P_b^{(24)}$ to $P_b^{(28)}$ are on the order of 10^{-6}, and $P_b^{(>28)} = \sum_{n>28} P_b^{(n)}$ is on the order of 10^{-6}.

Based on the above discussion, we may estimate the overall SER of this concatenated coding system when the inner LDPC code failure rate $P_l = 3.24 \times 10^{-6}$. According to (1), we first evaluate the overall SER when $m = 1$ (i.e., only one out of the v inner LDPC codeword decodings fails) as

$$\mathrm{SER}^{(m=1)} = \binom{v}{1} \times P_l \times (1-P_l)^{v-1} \times \left(\sum_{i>t} P_b^{(i)} \right) \tag{2}$$

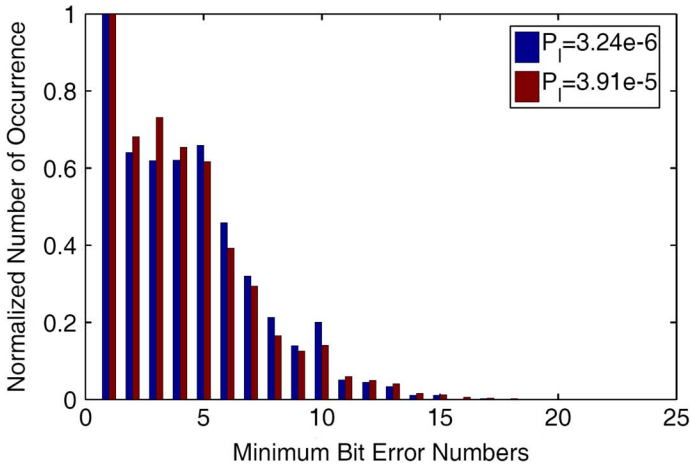

Fig. 2. Histogram representation of the data listed in Table II.

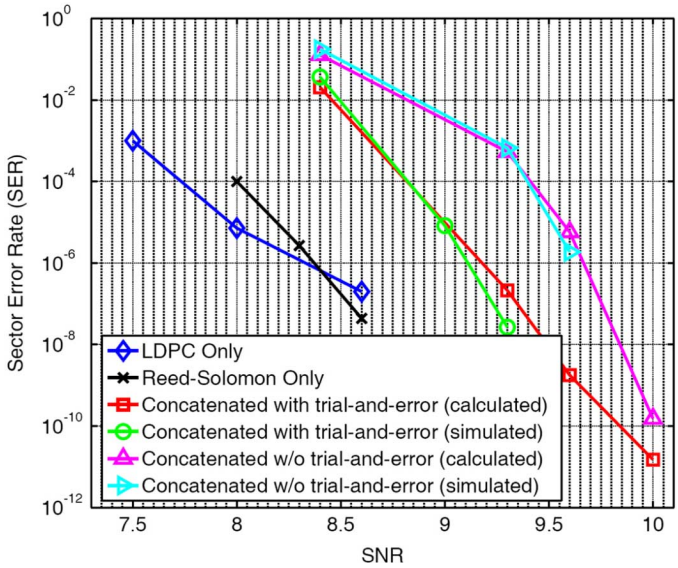

Fig. 3. SER performance comparison.

where $v = 8$ and $t = 28$, and we have that $\mathrm{SER}^{(m=1)}$ is on the order of 10^{-11}. For $m = 2$, we have

$$\mathrm{SER}^{(m=2)} = \binom{v}{2} \times P_l^2 \times (1 - P_l)^{v-2} \times S^{(m=2)} \qquad (3)$$

where

$$S^{(m=2)} = \sum_i \left(P_b^{(i)} \sum_{j > \max\{t-i,0\}} P_b^{(j)} \right).$$

Based on the data listed in Table II and the above conjectured $P_b^{(n)}$ for $n \geq 19$, we have that $\mathrm{SER}^{(m=2)}$ is on the order of 10^{-13}. Clearly, $\mathrm{SER}^{(m)}$ will drop sharply for $m > 2$, hence we can conclude that the overall SER of the concatenated coding system is on the order of 10^{-11} (i.e., dominated by the case when only one LDPC codeword decoding fails).

For the purpose of comparison, we further configured the FPGA-based simulator to investigate the performance when using LDPC-only and RS-only coding systems. This FPGA-based simulator can support the use of a regular rate-15/16 (32 768, 30 720) QC-LDPC code with the parity check matrix column weight of 4. The code parity check matrix contains an array of 2×32 circulant matrices, where all the circulant matrices have a column weight of 2 and are constructed randomly subject to the 4-cycle free constraint. This FPGA-based simulator can also support the use of a 4 kB rate-15/16 (2914, 2731, 91) RS code over $\mathrm{GF}(2^{12})$. We also considered the scenario that the proposed trial-and-error decoding strategy is not being used in the BCH-LDPC concatenated coding system. Finally, in order to further verify the SER estimation results, Monte-Carlo simulations of the BCH-LDPC concatenated coding system with and without trial-and-error decoding strategy are also obtained using the FPGA-based simulator.

Fig. 3 shows all the calculated and simulated SER results. It is clear that, under the 4 kB sector format, RS code has the best error-correcting performance (e.g., about 0.7 dB gain over this proposed BCH-LDPC concatenation). It should be pointed out that, if turbo equalization strategy (i.e., iterative detection and LDPC decoding) is being used, the performance of those LDPC-based schemes may be largely improved and potentially surpass RS code at increased silicon cost. A straightforward realization of turbo equalization with r global iterations may simply duplicate the detection/decoding datapath by r times. If we enable the use of decoding convergence check in LDPC decoding, the number of global iterations may change from one sector to the next. Such run-time variation of the number of global iterations may be potentially leveraged to reduce the silicon cost, which certainly deserves further investigation. Even without using the turbo equalization, as discussed in the following, the proposed BCH-LDPC concatenated coding system has less silicon cost than that of RS-only coding system, which may still make this concatenation option preferable in certain circumstances.

We further carried out ASIC design at 65 nm CMOS technology node in order to evaluate the silicon cost. With the RTL-level design entry using Verilog, we use Synopsys tool set and 65 nm CMOS standard cell library. The target read channel data rate is set to 1 Gbps. Following the min-sum LDPC decoder architecture presented in [18], we designed decoders for the rate-19/20 512-byte inner LDPC code and the rate-15/16 4 kB LDPC code. Notice that, due to the low inner LDPC code decoding failure rate, the trial-and-error concatenated code decoding can be readily handled by the hard disk controller. Hence we may not need to modify the inner LDPC code decoder in the read channel to support such trial-and-error decoding process. Following the architecture presented in [16], we designed an SOVA detector. To support the pipelining between the detector and decoder, an SRAM-based buffer should be used in between. For the design of BCH and RS code decoders, we assume the use of Berlekamp-Massey algorithm with the architecture as presented in [19]. Notice that the detector used in RS-only system is a Viterbi detector that is much simpler than its SOVA counterpart. The ASIC design results are summarized in Table III, which suggests that the concatenated coding system can have

less silicon cost compared with LDPC-only and RS-only coding systems.

V. Conclusion

This paper addressed a concatenated LDPC and BCH coding system design for magnetic recording read channel with a 4 kB sector format. Aiming to leverage the observed iteration-by-iteration bit error number oscillation behavior in case of LDPC code decoding failure, we propose a simple trial-and-error decoding strategy to improve the overall error correction capability. By implementing an FPGA-based read channel simulator, we have further demonstrated the ability to estimate the SER performance of such concatenated coding systems down to 10^{-11}. Finally, we evaluated the silicon cost advantage over other competing coding systems. This work suggests that such concatenated coding systems can be an attractive alternative in magnetic recording, which exploits the advantage of LDPC codes while circumventing the error floor concern. Future research is directed to investigating how the turbo equalization can be applied to reduce the coding gain gap with or even surpass the RS codes, and how the error-correcting performance comparison of these competing coding strategies will be impacted if burst defects are further taken into account.

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